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35 GHZ PSEUDOMORPHIC HEMT MMIC POWER AMPLIFIER[1]

D.W. Ferguson, S.A. Allen*, M.Y. Kao, P.M. Smith, P.C. Chao
M.A.G. Upton, and J.M. Ballingall

GE Aerospace, Electronics Laboratory
Syracuse, N.Y. 13221

*UC Santa Barbara, Santa Barbara, California.

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ABSTRACT

0.25μm gate-length double-heterojunction InGaAs Pseudomorphic HEMTs developed at the GE Electronics Laboratory have been integrated into a 3-stage power amplifier MMIC designed for the 34-36 GHz band. This first pass design exhibited a peak small-signal gain of 30 dB, minimum output power of 200 mW with 20 dB associated gain, power-added efficiency of greater than 18% and a return loss of greater than 14 dB over the entire band. This performance was measured with the MMIC operating from a single 6 Volt DC supply.

INTRODUCTION

In this paper we describe a successful first pass approach to HEMT MMIC design. Through the use of good modeling and low risk design techniques a 3-stage Pseudomorphic HEMT MMIC power amplifier was successfully produced in one design cycle, demonstrating state-of-the-art performance: small-signal gain peaked at 30 dB, minimum output power was 200 mW with 20 dB associated gain, power-added efficiency of greater than 17% and a return loss of greater than 14 dB over the entire band. To our knowledge this amplifier exhibits a combination of gain, efficiency and output power superior to that of any other previously reported MMIC over this band. In addition, the amplifier is compact, and requires only a single bias supply and a few off chip elements for operation.

AMPLIFIER DESIGN

The devices selected were 0.25μm pseudomorphic HEMTs because they have demonstrated excellent output power and efficiency at this frequency[1], and the 0.25μm gate length process can be fabricated with a high yield. The design goals of the amplifier were: 170 mW output power, 16 dB gain, 15% power-added efficiency, and 10 dB return loss from 34-36 GHz. With these goals in mind a three stage design based upon a 100, 200, and 400μm gate periphery chain was selected. These device sizes were incorporated into an initial device fabrication run so that the devices could be accurately characterized. This device run was performed prior to the design using several different wafers so that the variations in device parameters could be determined and a process-insensitive MMIC design could be developed.

The devices were characterized with DC measurements, power testing at 35 GHz, and on wafer S-parameter measurements. From this data, load line, small-signal models, bias conditions and power performance were predicted. The device models were obtained by using a six-via FET/wafer probe measurement technique[2], which provided excellent S-parameter data up to 40 GHz. This technique utilizes a TRL calibration on GaAs standards which calibrates at the device reference plane in a true microstrip environment, providing accurate data on the device exactly as it appears in the MMIC. Conventional co-planar probe data characterizes the device with incident co-planar fields which exhibit different parasitic effects as opposed to microstrip fields. In addition, a co-planar device requires added ground plane area, which can not be removed without affecting the device response. The accuracy of this method is demonstrated by the agreement between the small-signal model and measured data, which was excellent as can be seen in Figure 1.

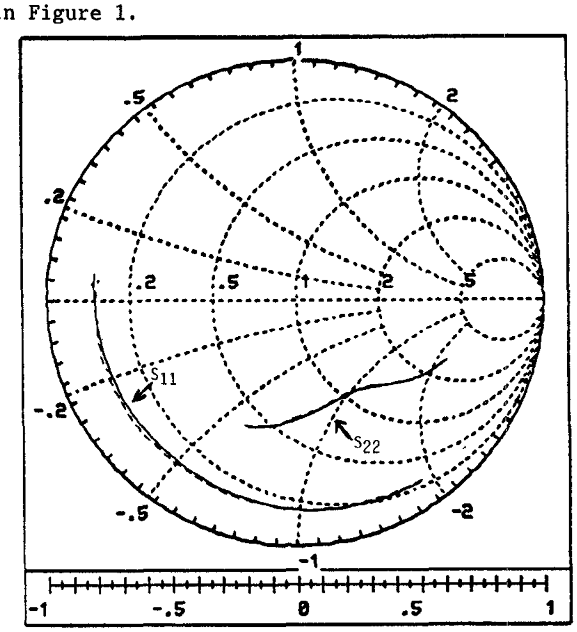

Figure 1 : Measured (- - -) and Modeled (-----) S-Parameters for a 200μm device using the Six-Via FET calibration process.

The amplifier design method was based upon a load line power matching technique[3] and used single open stub matching. Rather than use the bias injection lines as tuning elements, bias was injected through networks that were designed to have minimal effect on the circuit. This approach was taken in order to avoid the circuit elements in these networks having a large effect on the design since they are more difficult to model accurately at Ka Band. Device models taken from the different measured wafers were inserted into the circuit model in order to center the design. Preference was given to the wafers that performed best under power conditions, since these wafers were the more optimally processed samples. A circuit schematic of the amplifier is shown in Figure 2, and a photograph of the 2.8mm X 1.8mm MMIC is presented in Figure 3.

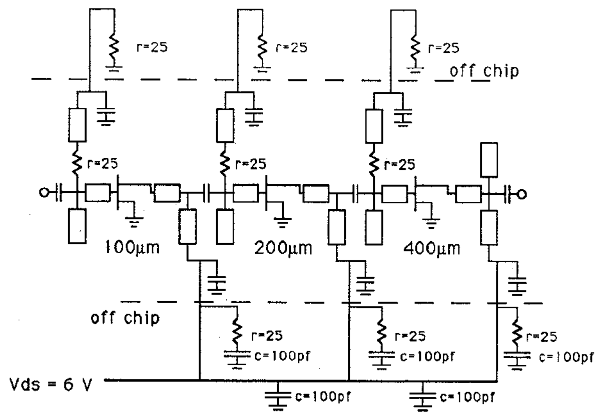

Figure 2 : Simplified schematic of the MMIC including off chip elements.

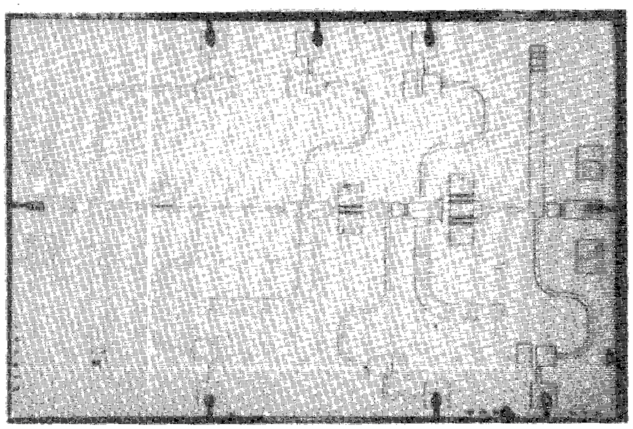

Figure 3 : Photo of a mounted MMIC. The circuit is 2.8mm X 1.8mm.

MEASURED PERFORMANCE

For RF testing the amplifiers were first mounted on a partially assembled waveguide test fixture and measured with an RF wafer prober for small-signal response. The fixtures were then assembled and the MMICs were power tested at individual frequencies over the band using a fixed frequency waveguide test setup.

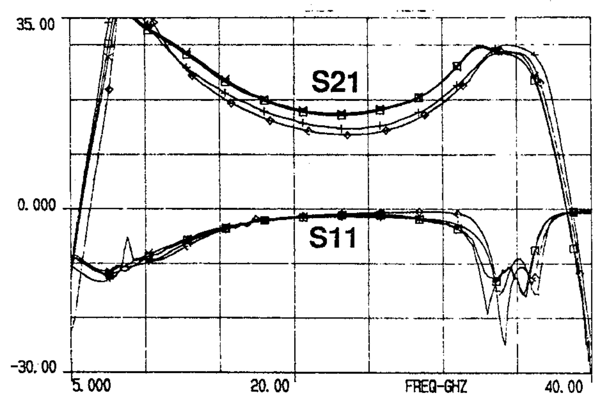

Figure 4 : Measured responses of four different MMIC's each from a different wafer. Peak small-signal gain was 30 dB.

Amplifiers fabricated on four different wafers demonstrated good performance tracking as seen in Figure 4. A maximum small-signal gain of 30 dB was measured. This is the highest gain ever reported for a MMIC at Ka Band. In addition, excellent agreement of measured with modeled small-signal response was obtained (as shown in Figure 5), as a result of the low risk MMIC design approach and accurate device characterization.

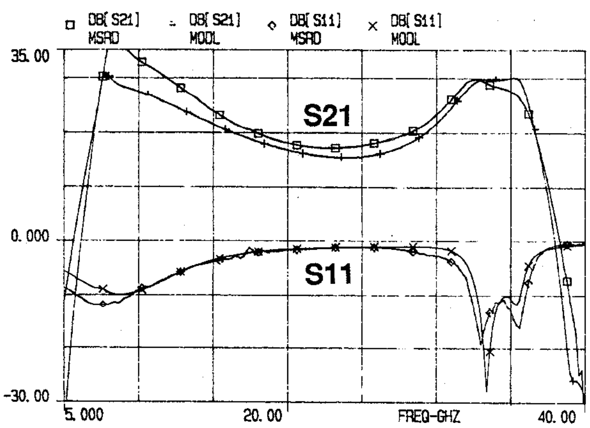

Figure 5 : Measured and Modeled small-signal amplifier response.

Although the amplifier was designed to allow for a +/- 50μm adjustment to the length of the input and output stubs, best performance was obtained when the stubs were adjusted to their nominal value, further verifying the accuracy of the design. Power performance with nominal stub lengths is shown in Figure 6. Peak power is 227 mW with 20 dB associated gain and 20.8% power-added efficiency at 35 GHz. Peak efficiency is 21.5% with 221 mW output power and 20 dB associated gain at 36 GHz. Linear gain ranged from 27 to 24 dB over the band. Under power drive return losses were excellent (better than 21 dB) and as the power drive was decreased values only as low as 14 dB were measured at 35 GHz. The amplifier also worked well below band: at 33 Ghz, 195 mW output power was measured with 20 dB gain and 17.5% efficiency.

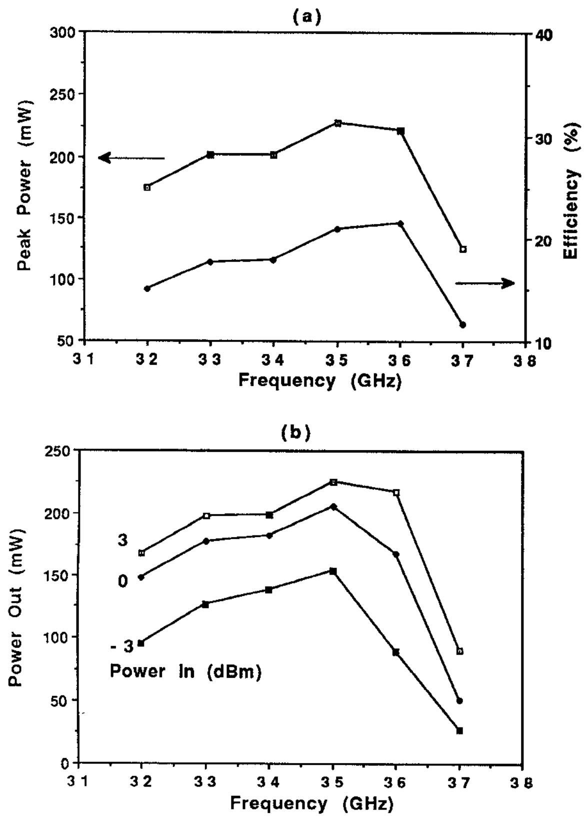

Figure 6 : Power performance of a MMIC with a single bias supply of 6V.
(a) Power and Efficiency vs Frequency.
(b) Power vs Frequency and Input Drive.

CONCLUSION

A comparison of these results with other published Ka Band single-chip MMIC performance data is shown in Figure 7. This work demonstrates a significant advance in monolithic technology. Although higher powers [5-7] and slightly higher efficiencies [2-3] have been demonstrated, this work represents the state-of-the-art in gain per stage (10 dB small-signal per stage at 34 GHz), and output power with high gain and efficiency (221 mW w/ 20 dB gain and 21.5% efficiency) from a single multi-stage circuit with a simple bias supply and a useful bandwidth. All of the higher power MMIC's exhibit very low gain due to the small number of stages, and typically have low efficiencies and/or narrow bandwidths. Multi-stage amplifiers present a more difficult design problem, since one must simultaneously design for gain, power and efficiency.

Reference	Freq. (GHz)	Gain (dB) Power/ Linear	Output Power (mW)	Power Added Efficiency (%)	Number of Stages
This work	36	20/24(30*)	221	21.5	3
[4]	32	14/16	90	25.9	2
[5]	34	16/21(26*)	112	21.6	3
[6]	34	3.8/6	200	21	1
[7]	28	7.2/8.2	560	15	2
[8]	33	2.8/5.2	600	8.5	1
[9]	30	3.3/3.6	2000	12	1

*** Measured at a different bias and/or frequency.**

Figure 7 : Comparison of Reported Power MMIC performance with this work.

It is also significant that this chip was designed within a single design cycle and successfully met all design goals, as can be seen in Figure 8. This demonstrates that low cost, low risk development of even high performance millimeter-wave MMIC's is possible with the use of proper device characterization, device modeling, and amplifier design techniques.

Parameter	Goal	Measured
Power Gain (dB)	16	20
Output Power (mW)	170	200
Efficiency (%)	15	17.7
Bandwidth (GHz)	34-36	33-36
Input Return Loss (dB)	10	14

Figure 8 : Comparison of design goals with achieved performance of the MMIC.

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